Overview

Feature

- Integrated ambient light sensor in one package
- Tiny 2mm × 1mm × 0.5mm module
- Convert ambient light intensity in 24 bit digital format
- Close to human eye response
- Wide configuration range
- V_{DD} wide operation range 1.7~2.0v
- 1.8V Power Supply with 1.8V~3.6V I^2C bus
- ELA2500 fully comply with current RoHS directives

Application

- Mobile phone for display management
- Wearable ambient light measurement

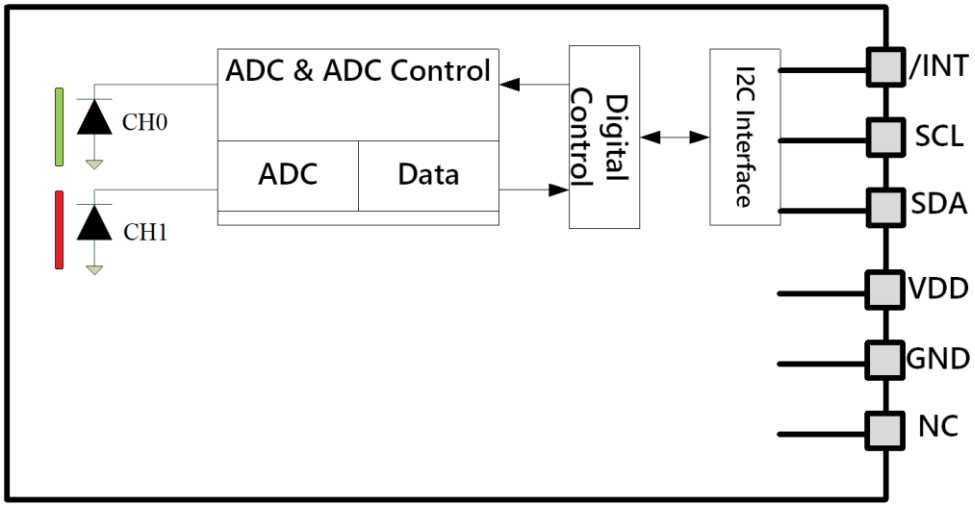
Description

The ELA2500 features ambient light measurement (ALS) with the extremely tiny 2mm × 1mm × 0.5mm module. This Device provides ambient light sensing for display management and backlight control.

The ELA2500 incorporates Photodiode, timing control and ADC into one chip and digital convert with I^2C interface. The ELA2500 provide the excellent spectral response that is close to human eye.

The ELA2500 has provided temperature calibration features and also has lower power design, including standby mode and wait mode support. The ALS and IR photodiodes have dedicated data converters producing 16-bit data. This architecture allows applications to accurately measure ambient light which enables devices to calculate illuminance to control display backlight.

Block Diagram



Pin Description

Description

Name	Pin No.	IO	Description
SDA	1	IO	IIC data (open drain)
INT	2	O	Interrupt pin (open drain)
NC	3	-	No connection
SCL	4	I	IIC clock
VDD	5	P	Power supply:1.7v~2.0v
GND	6	G	Ground

Electrical Specification

■ Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
VDD	Supply Voltage to GND	-0.3	2.0	V	
V_{IO}	Digital I/O Terminal Voltage	-0.3	3.6	V	
I_{IO}	Digital Output Terminal Current	-1	20	mA	
Electrostatic Discharge					
I_{SCR}	Input Current (latch-up immunity)	± 100		mA	Class II JEDEC JESD78E
ESD_{HBM}	HBM ElectrostaticDischarge	± 2000		V	JEDEC/ESDA JS-001-2017
ESD_{CDM}	CDM ElectrostaticDischarge	± 500		V	JEDEC JS-002-2014
Temperature Ranges and Storage Conditions					
T_{STRG}	Storage TemperatureRange	-40	85	˚C	
T_{BODY}	Package Body Temperature		260	˚C	IPC/JEDEC J-STD-020 The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices.”
RH_{NC}	Relative Humidity (non-condensing)		85	%	
P_{DISS}	Power Dissipation		50	mW	Average power dissipation over a 1 second period

■ Recommended Operation condition

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Supply Voltage to Sensor	1.7	1.8	1.98	V
f_{I2C}	Clock frequency of I^2C	-	-	400	Khz
T_A	Operating Ambient Temperature	-30		85	˚C

■ Electrical and optical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Active ALS State (PON=1) (1)		124		μA
		Idle State (PON=1)		23		
		Sleep State (PON = 0) (2)		0.5		
V_{OL}	INT, SDA output low voltage	6mA sink current			0.6	V
I_{LEAK}	Leakage current, SDA, SCL, INT		-5		5	μA
V_{IH}	SCL, SDA input high voltage(3)		1.26			V
V_{IL}	SCL, SDA input low voltage				0.54	V
T_{Active}	Time from power-on to readyto receive I^2C commands			1.5		ms

Note(s):

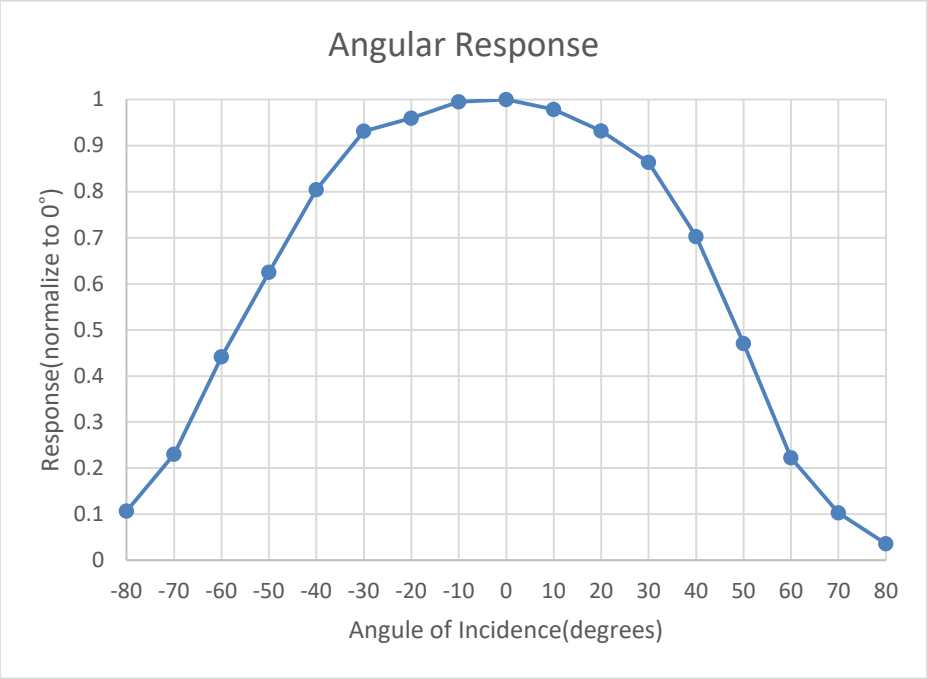
1. Active state occurs when PON =1 and the device is actively integrating ALS. For ALS, this time is determined by the ALS integration time (ATIME).
2. Sleep state occurs when PON = 0 and I²C bus is idle. If sleep state has been entered as the result of operational flow, SAI = 1, PON will remain high.
3. Digital pins: SDA, SCL, INT are tolerant to a communication voltage up to 3.6V

■ ALS optical characteristics

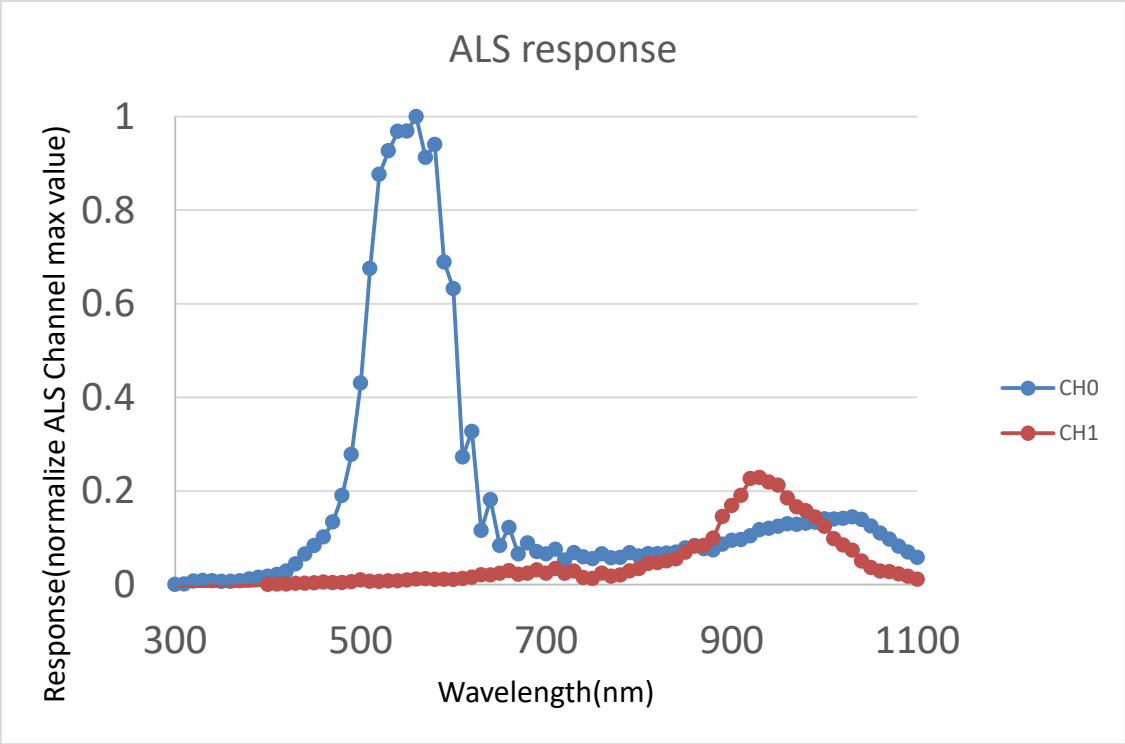
Parameter	Conditions	Min	Typ	Max	Unit
ALS sensitivity 1	6500K LED @ 500Lux AGAIN = 128x ATIME = 100ms	-15%	50105	+15%	Counts
ALS sensitivity 2	6500K LED @ 50Lux AGAIN = 1024x ATIME = 100ms	-15%	40100	+15%	Counts
ALS integration step size		2.746	2.78	2.815	ms
ALS dark count	0μW/cm^2 AGAIN = 1024x ATIME = 50ms	125	225	325	Counts
ALS 16x gain scaling	Relative to 128x		0.125		x
ALS 1024x gain scaling	Relative to 128x		8.5		x
ALS noise	AGAIN = 128x ATIME = 100ms		0.03		% (σ)

Typical Operating Characteristics

FOV



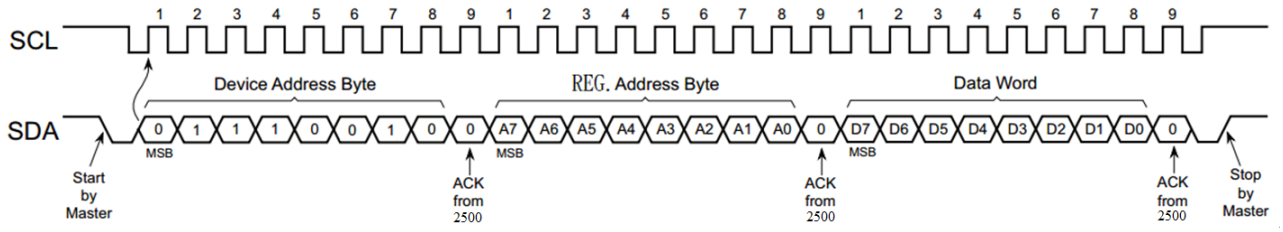
Spectrum



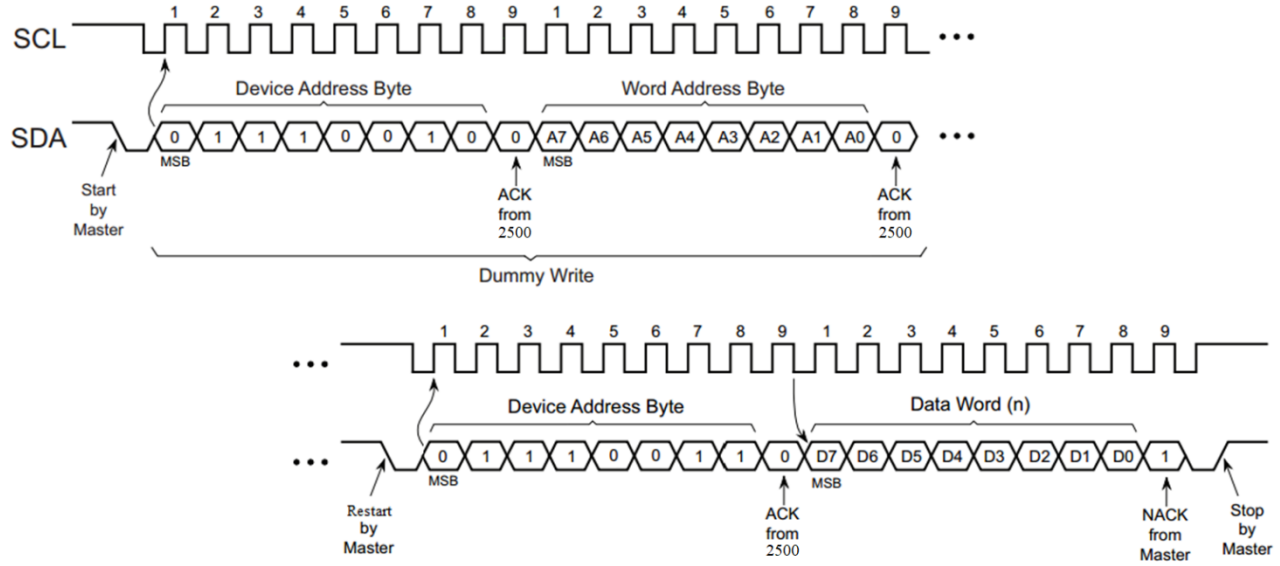
I2C Timing Diagram

IIC Communication

Write:



Read:



■ I2C address selection

Master I²C Bus Signal		7-Bit I²C Address
Clock	Data	
SCL	SDA	0x39
SDA	SCL	0x38

Notes:

A Single dummy I2C access (read or write with valid I2C stop) to the device is required to initialize the device their respective I2C address. The device will feedback a NOT-ACKNOWLEDGE (NACK) during initial dummy access.

Register Description

- Register table

Address	Register Name	R/W	Register Function	Reset Value
0x80	ENABLE	R/W	Enables states and interrupts	0x00
0x81	ATIME	R/W	ADC integration time	0x00
0x83	AWTIME	R/W	ALS wait time	0x00
0x84	AILTL	R/W	ALS interrupt low threshold low byte	0x00
0x85	AILTH	R/W	ALS interrupt low threshold high byte	0x00
0x86	AIHTL	R/W	ALS interrupt high threshold low byte	0x00
0x87	AIHTH	R/W	ALS interrupt high threshold high byte	0x00
0x8C	PERS	R/W	ALS interrupt persistence filters	0x00
0x8D	CFG0	R/W	Configuration zero	0x50
0x91	REVID	R	Revision ID	0x00
0x92	ID	R	Device ID	0x64
0x93	CFG1	R/W	Configuration one	0x68
0x94	STATUS	R, SC	Device status	0x00
0x95	ALSL	R	ALS (CH0) low data	0x00
0x96	ALSM	R	ALS (CH0) middle data	0x00
0x97	ALSH	R	ALS (CH0) high data	0x00
0x98	IRL	R	IR (CH1) low data	0x00
0x99	IRM	R	IR (CH1) middle data	0x00
0x9A	IRH	R	IR (CH1) high data	0x00
0xA6	REVID2	R	Revision ID two	0x00
0xA8	SOFTRST	R/W	Soft reset	0x00
0xAB	CFG3	R/W	Configuration 3	0x01
0xAE	CFG6	R/W	Configuration 6	0x3F
0xDD	INTENAB	R/W	Interrupt enables	0x00
0xF5	AS_CFG	R/W	ALS Configuration	0x18

Detail of Register Description

- *Enable register (Address 0x80)*

Addr: 0x80		Enable		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Reserved	0000	--	Reserved.
3	AWEN	0	RW	**ALS Wait Time Enable Flag** This bit active ALS wait feature which is set by AWTIME register AWEN = 1, ALS wait time is enabled. AWEN = 0, ALS wait time is disabled.
2	Reserved	0	--	Reserved.
1	AEN	0	RW	**ALS Enable Flag** AEN = 1, Ambient light function is enabled. AEN = 0, Ambient light function is disabled.
0	PON	0	RW	**Power On Enable Flag** This field activates the internal oscillator and ADC channels. Active high.

- *ATIME register (Address 0x81)*

Addr: 0x81		ATIME		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ATIME	0x00	RW	**ALS Integration Time Value** The ATIME value specifies the ALS integration time in 2.78msintervals. 0x00 indicates 2.78ms. The maximum ALS count value depends on the integration time.

Value	Integration Cycles	Integration Time	Maximum ALS Value
0x00	1	2.78ms	65535
0x01	2	5.56ms	131017
0x11	18	50.0ms	1179647
0x23	36	100ms	2359296
0x3F	64	178ms	4194304

				0xFF	256	712ms	16777215

- *AWTIME Register (Address 0x83)*

Addr: 0x83		AWTIME				
Bit	Bit Name	Default	Access	Bit Description		
7:0	AWTIME	0x00	RW	**ALS Wait Time Value** The AWTIME value specifies the ALS wait time in 2.78ms intervals. 0x00 indicates 2.78ms		
				Value	**Increments**	**Wait Time**
				0x00	1	2.78ms (33.4ms)
				0x01	2	5.56ms (66.7ms)
				0x11	18	50.0ms (600ms)
				0x23	36	100ms (1.20s)
				0x3F	64	178ms (2.14s)
				0xFF	256	712ms (8.54s)

- *AILTL Register (Address 0x84)*

Addr: 0x84		AILTL		
Bit	Bit Name	Default	Access	Bit Description
7:0	AILTL	0x00	RW	**ALS Low Threshold Value** This register sets the low byte of the LOW ALS threshold.

- *AILTH Register (Address 0x85)*

Addr: 0x85		AILTH		
Bit	Bit Name	Default	Access	Bit Description
7:0	AILTH	0x00	RW	**ALS Low Threshold Value** This register sets the high byte of the LOW ALSthreshold.

The ALS Low Threshold (AIL) is obtained by combining the AILTH and AILTL registers and left-shifting them by 8 bits to form a 24-bit threshold value.

- *AIHTL Register (Address 0x86)*

Addr: 0x86		AIHTL		
Bit	Bit Name	Default	Access	Bit Description

7:0	AIHTL	0x00	RW	**ALS High Threshold Value** This register sets the low byte of the HIGH ALS threshold.

- *AIHTH Register (Address 0x87)*

Addr: 0x87		AIHTH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	AIHTH	0x00	RW	**ALS High Threshold Value** This register sets the high byte of the HIGH ALSthreshold.

The ALS High Threshold (AIH) is obtained by combining the AIHTH and AITL registers and left-shifting them by 8 bits to form a 24-bit threshold value.

- *PERS Register (Address 0x8C)*

Addr: 0x8C		PERS			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:4	Reserved	0000	--	Reserved.	
3:0	APERS	0000	RW	This register sets the ALS persistence filter.	
				0 (0000)	Every ALS cycle
				1 (0001)	Any value outside ALS thresholds
				2 (0010)	2 consecutive ALS values out of range
				3 (0011)	3 consecutive ALS values out of range
				4 (0100)	5 consecutive ALS values out of range
				5 (0101)	10 consecutive ALS values out of range
				6 (0110)	15 consecutive ALS values out of range
				7 (0111)	20 consecutive ALS values out of range
				...	...
				13 (1101)	50 consecutive ALS values out of range
				14 (1110)	55 consecutive ALS values out of range
				15 (1111)	60 consecutive ALS values out of range

- *CFG0 Register (Address 0x8D)*

Addr: 0x8D		CFG0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**

7:3	Reserved	01010	--	Reserved. **Must be set to default value.**
2	AWLONG	0	RW	**ALS Wait Long Flag** The AWTIME is increased by a factor of 16 when AWLONG is asserted. AWLONG = 1, AWTIME = AWTIME x 16 AWLONG = 0, AWTIME = AWTIME x 1
1:0	Reserved	00	RW	Reserved. **Must be set to default value.**

■ REVID Register (Address 0x91)

Addr: 0x91		REVID		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	Reserved	00000	RO	Reserved.
2:0	REV_ID	000	RO	Device revision number.

■ ID Register (Address 0x92)

Addr: 0x92		ID		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:2	ID	011001	RO	Device type identification.
1:0	Reserved	00	RO	Reserved.

■ CFG1 Register (Address 0x93)

Addr: 0x93		CFG1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	Reserved	011	RW	Reserved. Must be set to default value.
4:0	AGAIN	01000	RW	This field sets the gain of the ALS sensor. **ALS Gain Value** AGAIN = 8, 128x gain. AGAIN = 11, 1024x gain.

■ STATUS Register (Address 0x94)

Addr: 0x94		STATUS Register		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**

7	ASAT	0	R, SC	Analog saturation flag signals that the ALS results may be unreliable due to saturation of the AFE.
6:5	Reserved	00	--	Reserved.
4	AINT	0	R, SC	ALS interrupt flag indicates that ALS results (CH0) have exceeded thresholds and persistence settings.
3:0	Reserved	0000	--	Reserved.

- ALSL Register (Address 0x95)

Addr: 0x95		ALSL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ALSL	0x00	RO	**ALS Channel 0 Low Byte Data** This register contains the low byte of the 24-bit ALSchannel (CH0) data.

- ALSM Register (Address 0x96)

Addr: 0x96		ALSM		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ALSM	0x00	RO	**ALS Channel 0 Middle Byte Data** This register contains the middle byte of the 24-bit ALS channel (CH0) data.

- ALSH Register (Address 0x97)

Addr: 0x97		ALSH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ALSH	0x00	RO	**ALS Channel 0 High Byte Data** This register contains the high byte of the 24-bit ALSchannel (CH0) data.

- IRL Register (Address 0x98)

Addr: 0x98		IRL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	IRL	0x00	RO	**ALS Channel 1 low Byte Data**

				This register contains the low byte of the 24-bit IR channel (CH1) data.

■ IRM Register (Address 0x99)

Addr: 0x99		IRM		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	IRM	0x00	RO	**ALS Channel 1 Middle Byte Data** This register contains the middle byte of the 24-bit IR channel (CH1) data.

■ IRH Register (Address 0x9A)

Addr: 0x98		IRH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	IRH	0x00	RO	**ALS Channel 1 High Byte Data** This register contains the high byte of the 24-bit IRchannel (CH1) data.

■ REVID2 Register (Address 0xA6)

Addr: 0xA6		REVID2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Reserved	0000	R	Reserved.
3:0	VER_ID	0000	R	Device version number.

■ SOFTRST Register (Address 0xA8)

Addr: 0xA8		SOFTRST		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:2	Reserved	000000	--	Reserved. **Must be set to default value.**
1	POR	0	RW	**Power On Reset Enable Flag** Writing a 1 to this bit will cause a power on reset. This will immediately terminate all device operation and put the device into the sleep state.

0	SOFTRST	0	RW	**Software Reset Enable Flag** Writing a 1 to this bit will cause all registers to bereset to their default state. This will immediately terminate all device operation and put the device into the sleep state.

■ CFG3 Register (0xAB)

Addr: 0xAB		CFG3		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	INT_READ_CLEAR	0	RW	**Status Reset Flag** If set, then flag bits in the STATUS register will be reset whenever the STATUS register is read over I^2C.
6:5	Reserved	00	--	Reserved. Must be set to default value.
4	SAI	0	RW	**Sleep After Interrupt Enable Flag** The Sleep After Interrupt bit is used to place the device into a low power mode upon an interrupt pinassertion.

PON	**SAI**	**INT**	**Oscillator**
0	X	X	OFF
1	0	X	ON
1	1	1	ON
1	1	0	OFF

3:0	Reserved	0001	--	Reserved. **Must be set to default value.**

■ CFG6 Register (0xAE)

Addr: 0xAB		CFG3		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	AGC	0	RW	**Auto Gain Control** AGC = 0, AGC is disabled. AGC = 1, AGC is enabled.
6:0	Reserved	0111111	--	Reserved. **Must be set to default value.**

■ INTENAB Register (Address 0xDD)

Addr: 0xDD	INTENAB

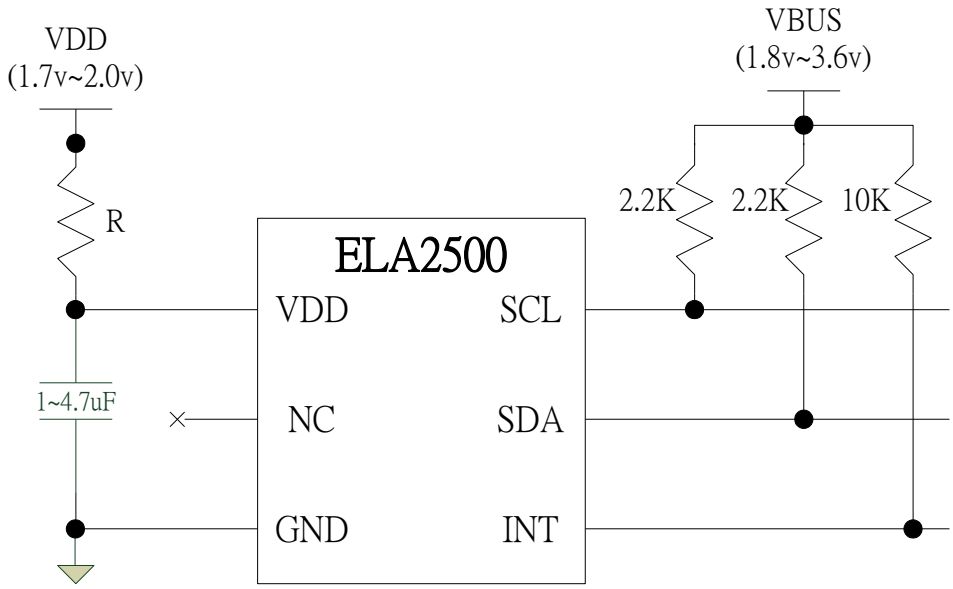
Bit	Bit Name	Default	Access	Bit Description
7	ASIEN	0	RW	ALS Saturation Interrupt Enable
6:5	Reserved	00	--	Reserved.
4	AIEN	0	RW	ALS Interrupt Enable
3:0	Reserved	0000	--	Reserved. **Must be set to default value.**

- AS_CFG Register (Address 0xF5)

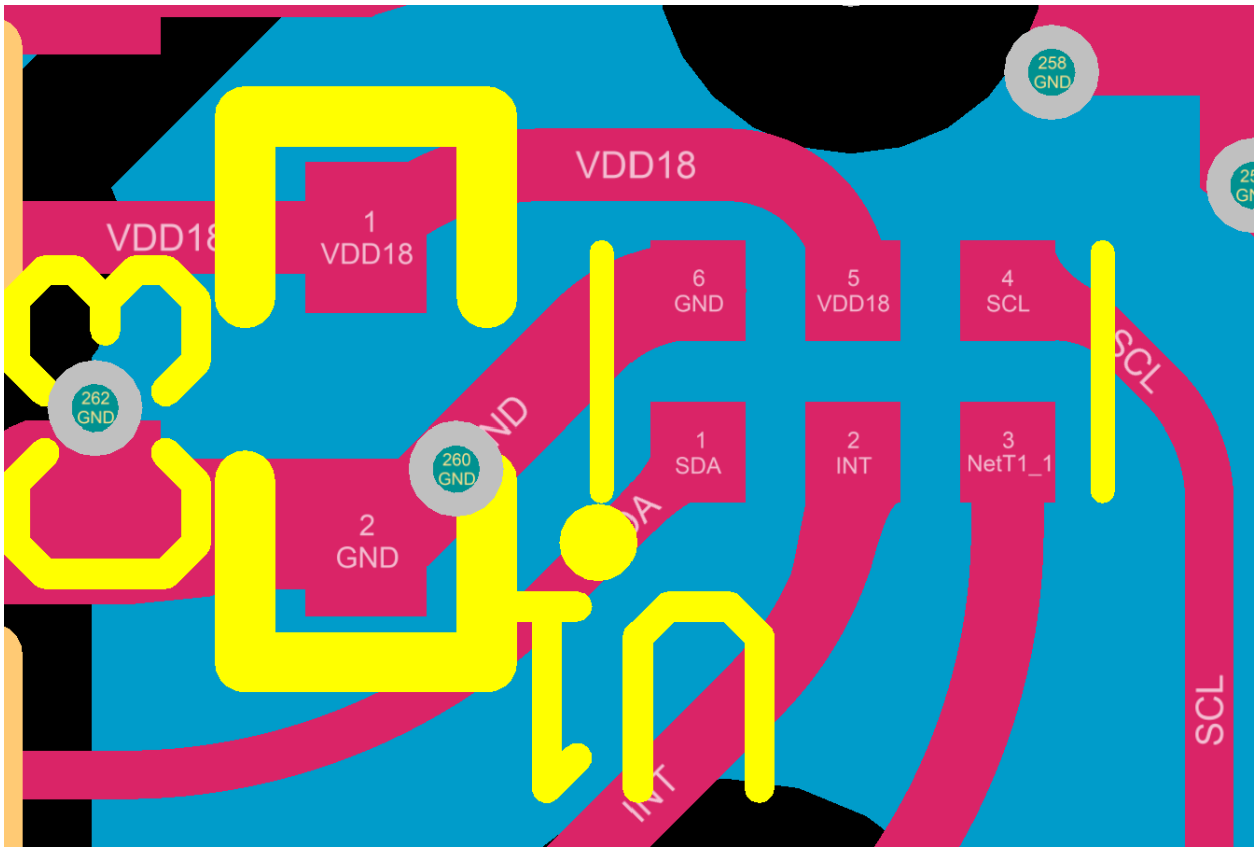
Addr: 0xF5		AS_SWCFG				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**		
7:2	Reserved	000110	--	**Must be written as 000100.**		
1:0	CITGTIME	00	RW	ALS Integration Time Value		
				CITGTIME	Integration Cycle	Integration Time(us)
				0	8/8	2774
				1	Reserved	Reserved
				2	1/8	344
				3	1/64	44

The CFG1 Register bit4 to bit0 set as"01000", if CITGTIME[1:0]=0, AGAIN=128X, else if CITGTIME[1:0]=2, AGAIN=16X, else CITGTIME[1:0]=3, AGAIN=2X

Application Note

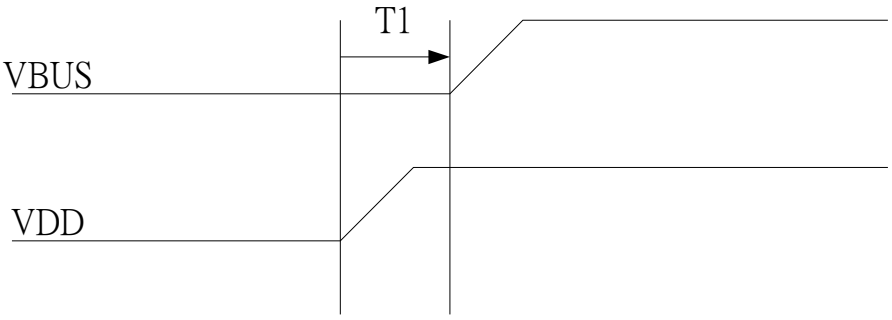


Note: The recommended R value is 22 ohm



Recommended Circuit Layout

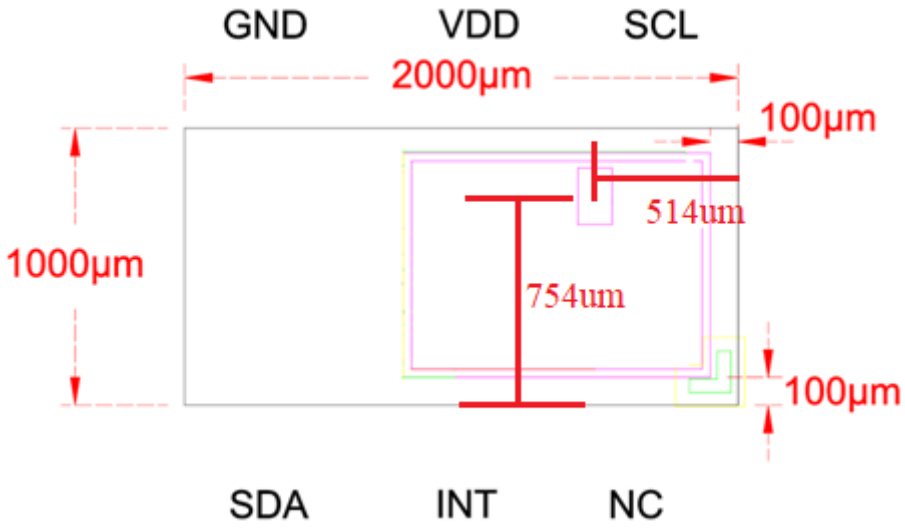
- Power on Sequence



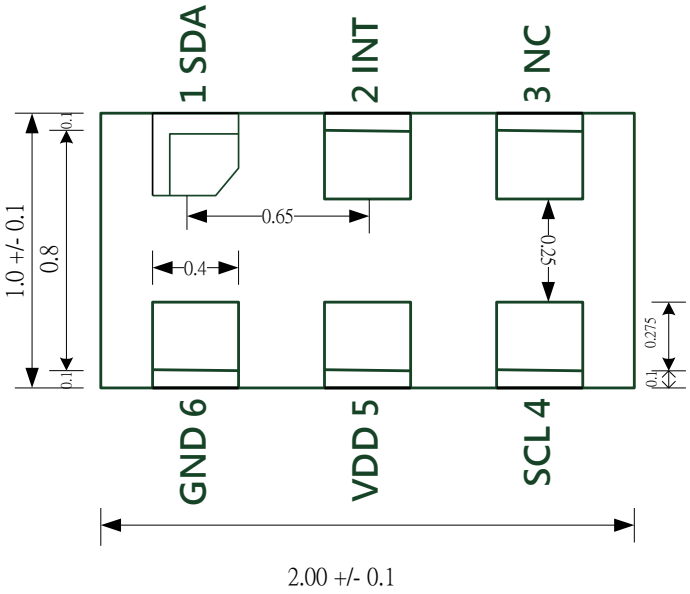
Note: The T1 time is recommended more than 30ms (VDD first is recommended)

Package

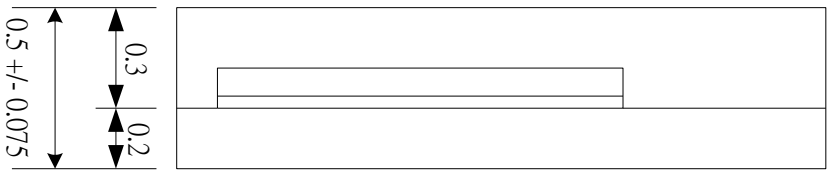
- Top View



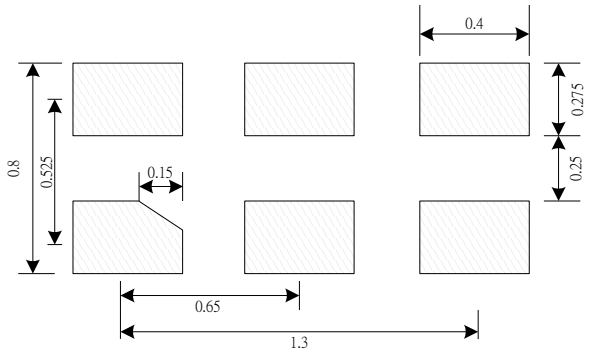
- Bottom View



- Side View

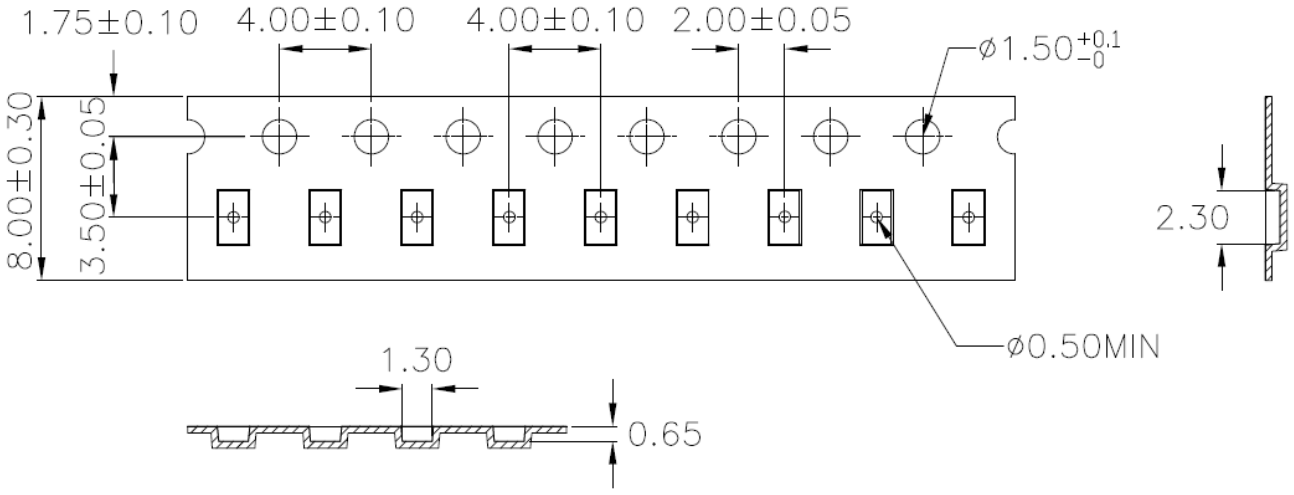


- Recommended PCB Layout

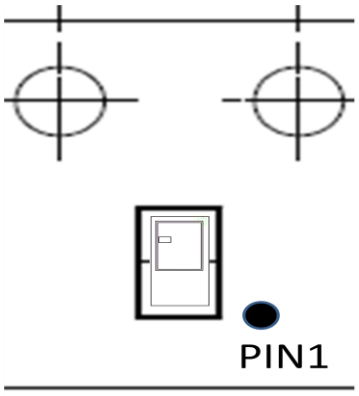


Note: all dimensions are in mm

Tape and Reel Information



Chip in Reel



Note: all dimensions are in mm

Order & Packing Information

Package	Product ID	Packing
OPLGA 2x1x0.5mm	ELA2500GP06NDR	Tape & Reel 3K pcs

GP06: OPLGA 2x1x0.5mm 6PIN

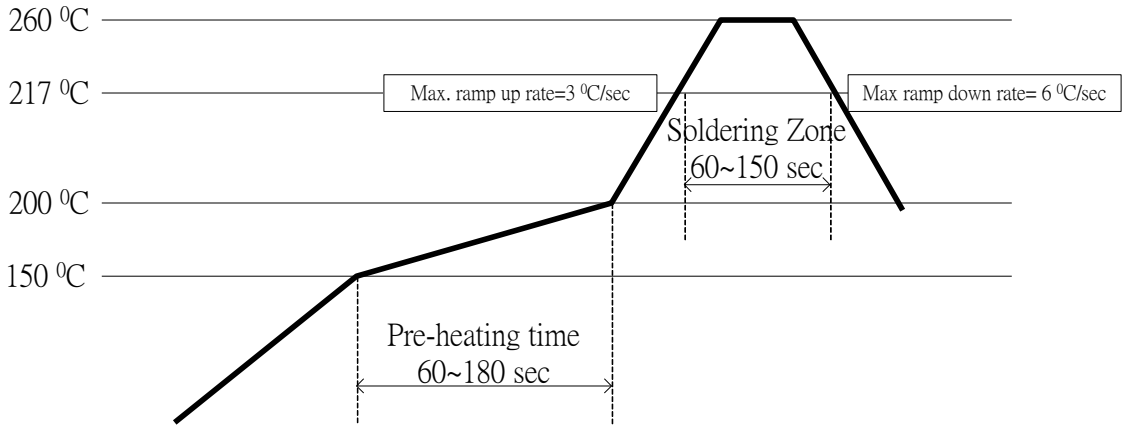
N: RoHS & Halogen free

D:-30~85℃

R:Tape & Reel

Soldering Information

■ Soldering condition



Note [1]: Reflow soldering should not be done more than three times

Note [2]: When soldering, do not stress on IC during heating

Note [3]: After soldering, do not warp the board

Recommended of storage method and ESD precaution

Dry box storage is recommended as soon as the aluminum bag has been opened. It could prevent moisture absorption.
The following conditions should be followed if dry boxes are not available

-- Storage temperature 10C to 30C
-- Storage humidity <= 60% RH max

After more than 72 hours Under the conditions moisture content will be too high for reflow soldering. In case of moisture absorption, the devices will recover to former conditions by drying under the following condition

-- 192 hours at 40C and 5% RH or
-- 96 hours at 60C and < 5% RH for device containers, or
-- 24 hours at 125C is not suitable for reel

ESD precaution
-- When the Chips are removed from Anti-static bag, please follow the handing procedure to prevent ESD damage